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(54) **Telephone line extenders**

(57) Apparatus suitable for compensation of a transmission line, particularly a telephone line in an automatic telephone system, the apparatus including a plurality of compensating networks 104–107 having reactive components and a control, switching, and measuring system which measures the loss of the line with each network connected to it in turn, retains a record of the network providing the best result, and connects that network to the line. The apparatus performs the test sequence each time the subscriber's telephone is lifted. The best network is selected by comparing the networks in pairs and retaining in memory 13 a record of the better result at each comparison, the retained result being used as one of the pairs in the subsequent comparison.

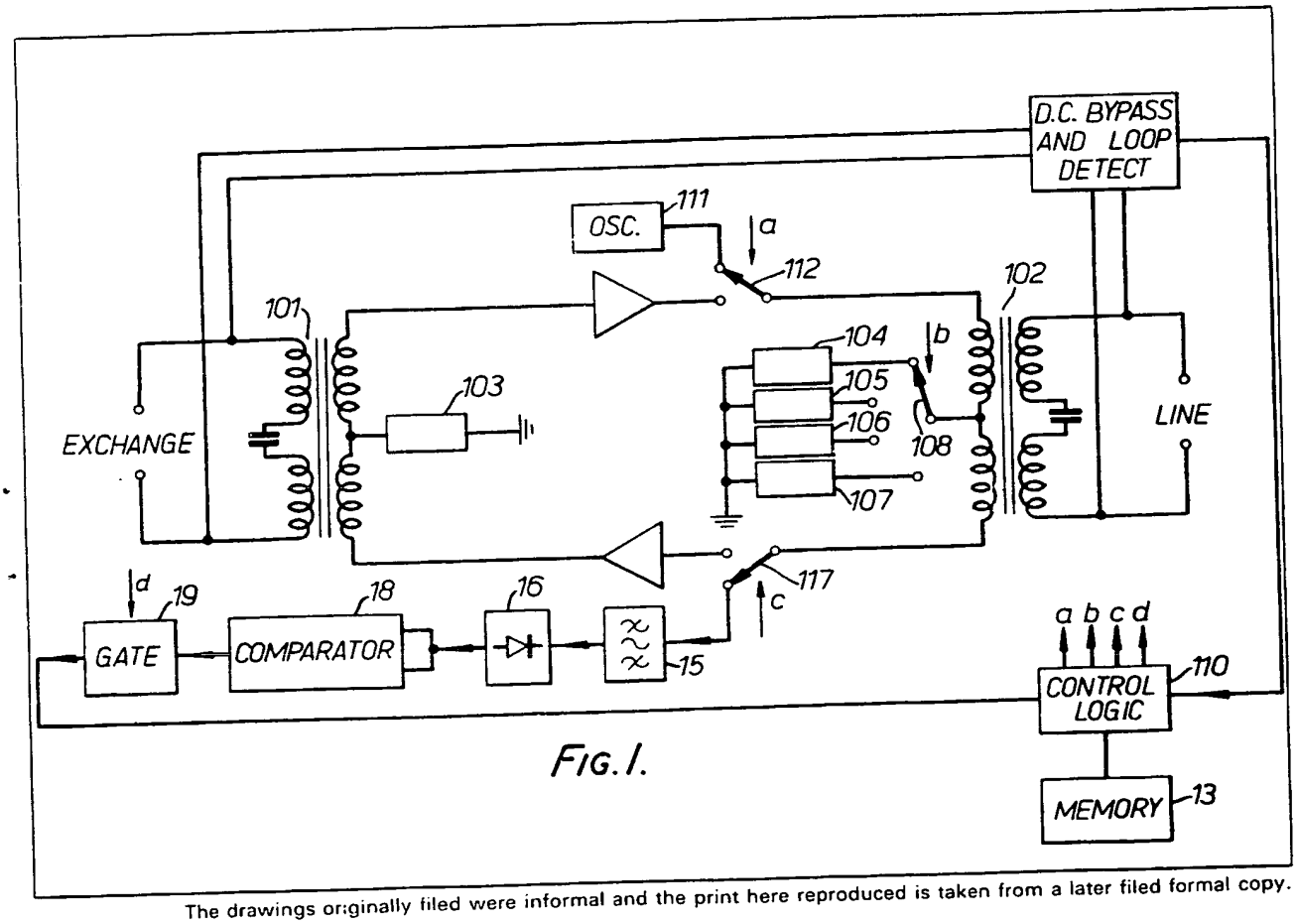

FIG. 1.

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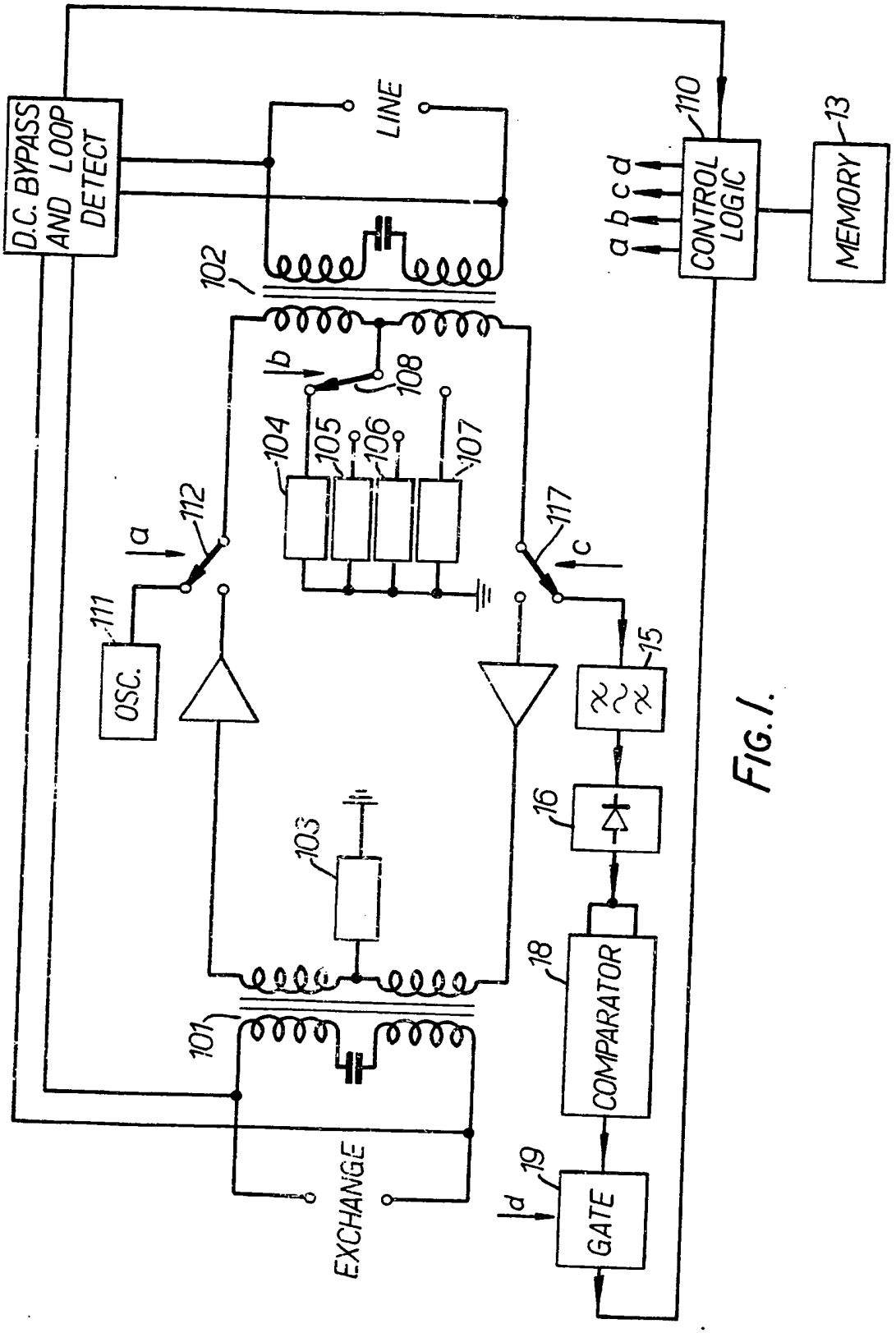
D.C. BYPASS AND LOOP DETECT
LINE
110
CONTROL LOGIC
MEMORY
13
a b c d
102
b
108
104
105
106
107
112
a
117
c
111
OSC.
15
103
16
18
COMPARATOR
101
EXCHANGE
19
d
GATE

FIG. 1.

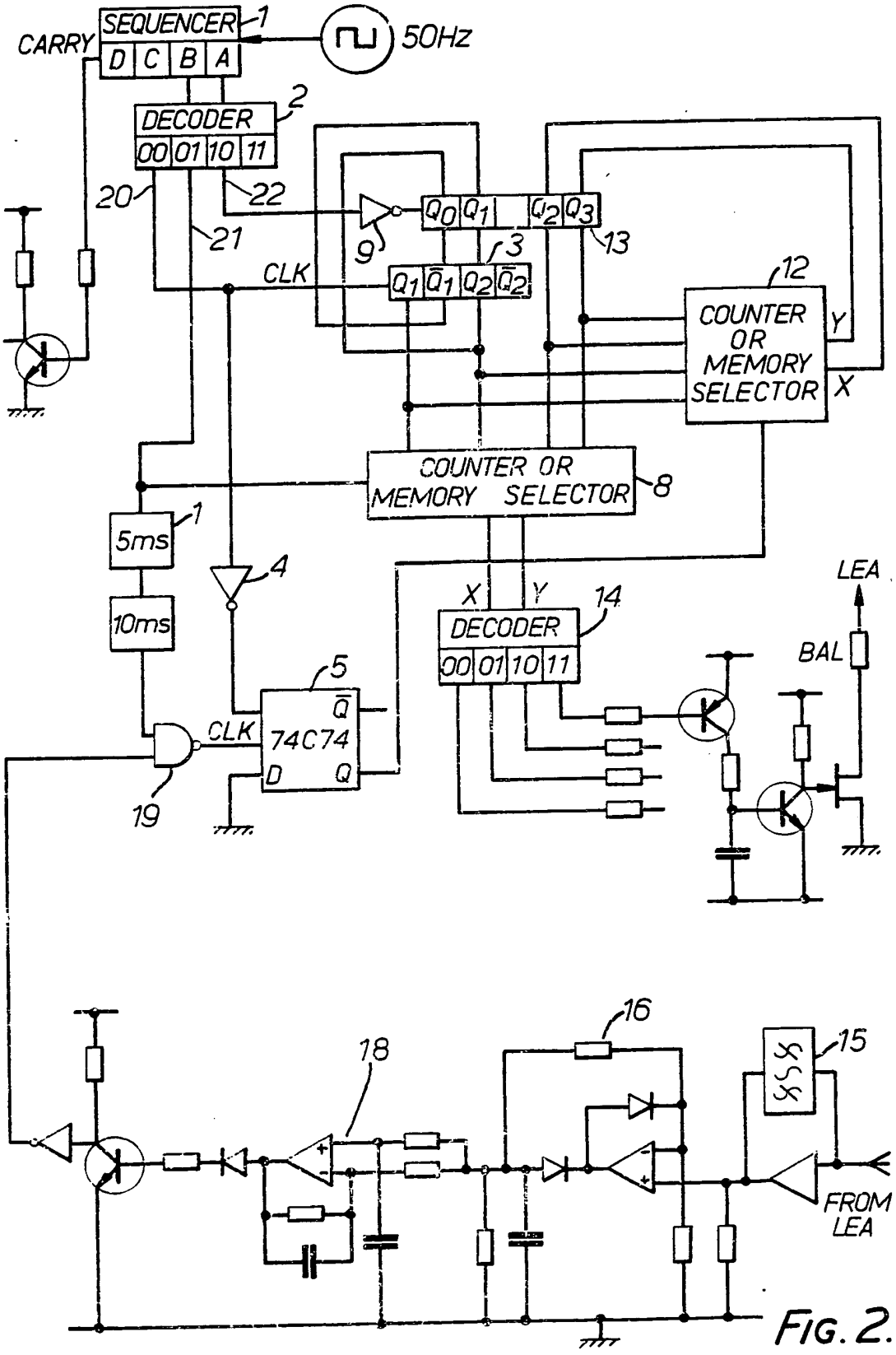
SEQUENCER
1
CARRY
D C B A
50Hz
DECODER
2
00 01 10 11
20
22
21
9
Q0 Q1 Q2 Q3
13
3
CLK
Q1 Q̄1 Q2 Q̄2
12
COUNTER OR MEMORY SELECTOR
Y
X
COUNTER OR MEMORY SELECTOR
8
5ms
1
10ms
4
X
Y
14
DECODER
00 01 10 11
LEA
BAL
5
Q̄
CLK
74C74
D
Q
19
16
18
15
FROM LEA

FIG. 2.

3,74

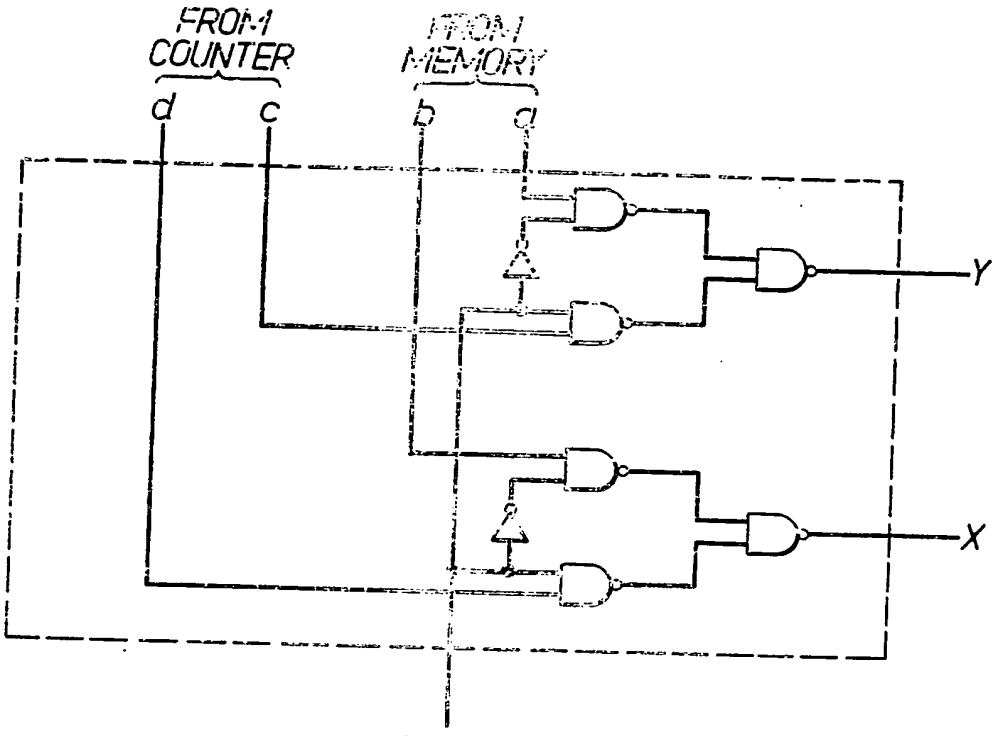

FIG. 3.

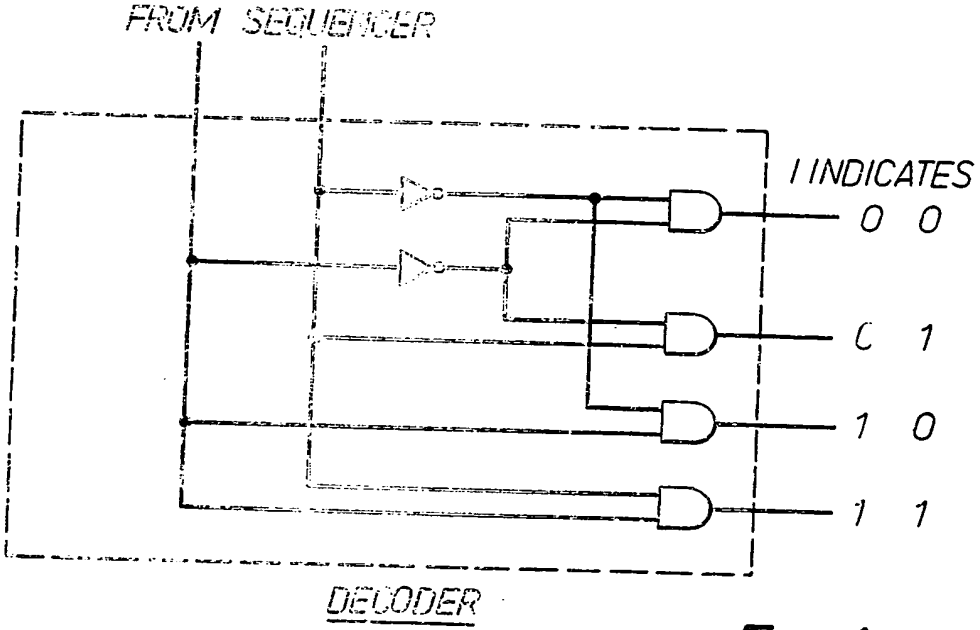

FIG. 4.

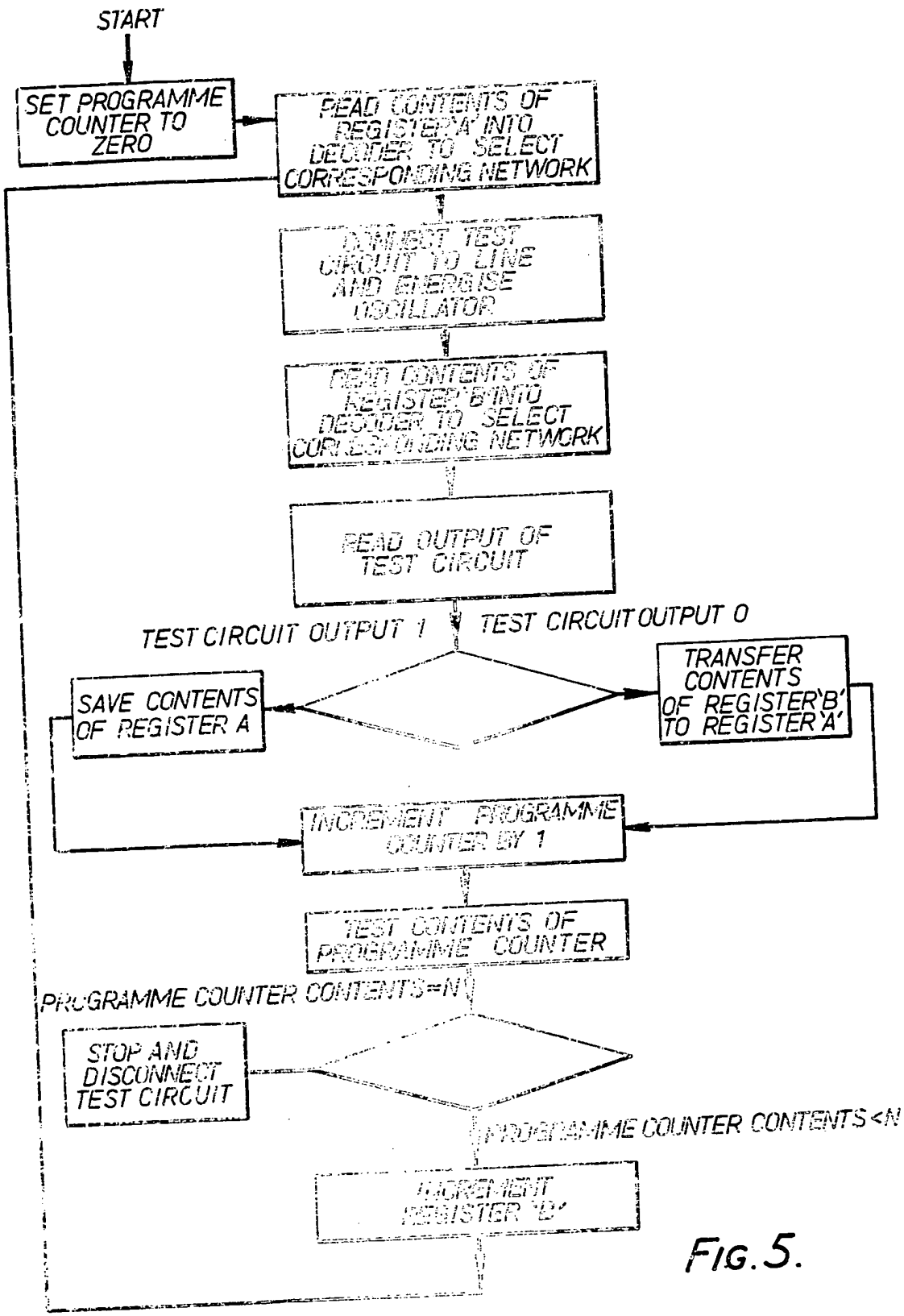
START
SET PROGRAMME COUNTER TO ZERO
READ CONTENTS OF REGISTER 'A' INTO DECODER TO SELECT CORRESPONDING NETWORK
CONNECT TEST CIRCUIT TO LINE AND ENERGISE OSCILLATOR
READ CONTENTS OF REGISTER 'B' INTO DECODER TO SELECT CORRESPONDING NETWORK
READ OUTPUT OF TEST CIRCUIT
TEST CIRCUIT OUTPUT 1
TEST CIRCUIT OUTPUT 0
SAVE CONTENTS OF REGISTER A
TRANSFER CONTENTS OF REGISTER 'B' TO REGISTER 'A'
INCREMENT PROGRAMME COUNTER BY 1
TEST CONTENTS OF PROGRAMME COUNTER
PROGRAMME COUNTER CONTENTS=N
STOP AND DISCONNECT TEST CIRCUIT
PROGRAMME COUNTER CONTENTS<N
INCREMENT REGISTER 'B'

FIG. 5.

SPECIFICATION

Improvements in and relating to telephone line extenders

The invention relates to line extender apparatus for telephone systems.

In telephone systems, some subscribers' installations are located at such distances from the exchange that special measures need to be taken to ensure reliable operation of both the signalling and transmission equipment in the system. Equipment used to achieve these purposes are known as line extenders (signalling) and line extenders (audio), respectively. The present invention relates to line extenders (audio).

Line extender apparatus assists in reliable operation by providing compensation for resistive and reactive components of a transmission line which connects subscribers to an exahange. Because transmission lines connecting subscribers to exchanges are likely to be all of different lengths, they represent a wide range of complex loads and make it advantageous to provide adjustable reactive and resistive components in line extender apparatus intended to provide full compensation for any line. When automatic operation is contemplated the inclusion of adjustable reactive components in the line extender apparatus leads to unacceptably complicated apparatus. A need exists, therefore, for line extender apparatus which avoids the complexity of adjustable reactive components systems and which is suitable for automatic operation.

It is an object of the present invention to provide line extender apparatus suitable for automatic telephone systems.

According to the invention apparatus for compensation of a transmission line includes a plurality of compensating networks having reactive components arranged for connection to the transmission line, and means arranged to measure, periodically, a parameter of the transmission line with one of the networks connected to it and to connect one of the compensating networks to the transmission line according to the value of the parameter.

The compensating networks may be connected to first switch means which is arranged to connect one of the compensating networks to the line in accordance with a code which is applied to the first switch means.

The code may be generated by means of a control circuit which is arranged to provide the code in accordance with the measured value of the parameter. The control circuit may have a digital data store connected to it for storing the said code.

Means arranged to measure a parameter of the transmission line may include an oscillator, a test circuit, and second switch means arranged to interrupt the transmission line periodically to connect the oscillator and test circuit to the transmission line.

The test circuit may include an analogue memory device and a comparator arranged to compare the result of each parameter measurement with the immediately preceding value.

The apparatus for compensation of a transmission line may be arranged to test the parameter of the transmission line with two randomly selected networks in sequence, and to select the network giving the better result as the balance network for the line.

Alternatively, the apparatus for compensation of a transmission line may be arranged to test the parameter of the transmission line with all possible combinations of networks in sequence, and to select the network giving the best result as the network for the line.

The test circuit may include a differential amplifier arranged as a comparator having a long time-constant input port and a short time-constant input port. In a telephone network, the parameter measured may be the trans-hybrid loss measured at the hybrid transformer.

Apparatus for compensation of a transmission line according to the invention will now be described by way of example only and with reference to the accompanying drawings, in which:

Figure 1 is a block schematic representation of apparatus for the compensation of a telephone line connected to the transmission port of the central office equipment of a telephone system,

Figure 2 is a detailed block schematic representation of a logic network and memory included in Fig. 1,

Figure 3 is a detailed schematic representation of a selector circuit included in Fig. 2,

Figure 4 is a detailed schematic representation of a decoder circuit included in Fig. 2, and

Figure 5 is a flow diagram representation of the functions carried out by the system of Fig. 2.

Fig. 1 shows a first audio frequency transformer 101 available for connection to an exchange transmission line, and a second audio frequency transformer 102 available for connection to a subscriber's transmission line. The centre-tap of the first transformer 101 is connected to a network 103, and four networks 104, 105, 106 and 107 are connected to respective terminals of a switch arrangement 108 by means of which any one of the four networks 104, 105, 106 and 107 is connectable to the centre-tap of the second transformer 102. The network connected to the centre-tap of the second transformer 102 must be selected so as to compensate for the effects caused by connection of a subscriber's line to the second transformer 102.

The switch 108 is an electronic switching arrangement, in practice, but is indicated

functionally in Fig. 1.

A memory 13 is included in the system. The memory 13 records the data necessary to select one of the networks 104, 105, 106 or 107 by way of a control logic network 110, and may retain a record of the data when the subscriber's telephone is not in use. When the subscriber's telephone is next lifted off the hook, the balance network next in sequence becomes connected in circuit, and an audio oscillator 111 is connected in the "send" path of the system by way of a switch 112, and a test circuit is connected in the "receive" path of the system in order to measure the loss at the second transformer 102. The test circuit is connected by way of a switch 117.

The test circuit consists of a bandpass filter 15, a precision rectifier 16, a comparator 18, and a gate circuit 19. The bandpass filter 15 is connected between the second transformer 102 and the precision rectifier 16, and the input port of the comparator 18 is connected to the output port of the precision rectifier 16. The comparator 18 is divided into a short time-constant section and a long time-constant section which are arranged in parallel with each other. The gate circuit 19 is connected to the output port of the comparator 18, and is connection also to the control logic network 110 so as to control its state in association with the memory 13.

The transmission line balancing apparatus operates as follows:—

While the subscriber's telephone is on the hook the memory 13 will contain data indicating which of the balance networks 104, 105, 106 and 107 is considered to provide the highest loss at the second transformer 102. This represents the "present best balance" condition. When the teleohone is lifted off the hook the balance network next in sequence is connected in circuit, the oscillator 111 is connected into the "send" path of the system by the switch 112 and the loss is measured at the second transformer 102.

The more detailed circuit diagram shown in Fig. 2 is the control logic part of a system which operates with a test signal of about 1500 Hz. The 1500 Hz test oscillator is not shown in Fig. 2, but it is within the skill of a person trained in the art to provide a suitable test oscillator using discrete components, TTL or MOS logic gates, or the like. Alternatively, an integrated circuit oscillator based on an NE 555 integrated circuit may be employed.

In Fig. 2, a 50 Hz square wave signal derived from a separate oscillator output signal is applied to a code generator 1 which is arranged to generate a two-digit binary sequence, starting with 00 and ending with 11, and then to switch off the test oscillator. The code generator 1 is activated by the subscriber's telephone being lifted off the hook. In this way, the control logic repeats the same sequence of actions each time the subscriber's telephone is lifted off the hook.

The code generator 1 controls a first binary decoder 2 which provides a logic "1" output signal on only one of four output ports according to the binary code applied to its input ports. The combined function of the code generator 1 and the binary decoder 2 is generally similar to the function of a ring counter. The output port 20 of the binary decoder 2 is connected to the CLOCK input port of a dual D bistable flip-flop 3 and to the input port of a first inverter 4 which has its input port connected to the PRESET input terminal of a single D bistable flip-flop 5. The output port 20 of the binary decoder 2 is the output port which provides a logic 1 output level when the decoder input code is 00.

The output port 21 of the binary decoder 2 is connected to a monostable flip-flop 7 and to a first selector circuit 8. The output port 21 of the binary decoder 2 provides a logic 1 when the decoder input code is 01. The output port 22 of the binary decoder 2 is connected to the input port of a second inverter 9, the output port of the second inverter 9 being connected to the control input port of a four-bit memory 13. The control input port of the memory 13 controls the entry of data into the memory 13. The memory 13 has a left pair of input ports associated with a left pair of output ports, and a right pair of input ports associated with a right pair of output ports. The control input port of the memory 13 is identified as the $\overline{\text{SAVE}}$ input port, and data is accepted by the memory 13 only when its $\overline{\text{SAVE}}$ input port is taken to logic 0.

A second selector circuit 12 having first and second pairs of input ports and a pair of output ports is provided. This second selector circuit 12 is arranged with the first pair of input ports connected to the Q1, Q2 output ports of the dual D bistable flip-flop 3, the second pair of input ports connected to the right pair of output ports of the memory 13, and its input ports connected to the right pair of input ports of the memory 13. The second selector circuit 12 is also provided with a control input port which controls the connection of either the first or the second pair of input ports to the output port.

The dual D bistable flip-flop has its data input ports connected to the left output ports of the memory 13, and its $\overline{Q1}$, Q2 output ports connectd to the left input ports of the memory 13 with the bits interchanged. This feedback arrangement is a "twist and invert" loop by means of which a two-bit word taken from the dual D bistable flip-flop 3 back to the memory 13 is returned to the dual D bistable flip-flop 3 with the bits interchanged and one bit inverted. For example, if the binary word 00 is stored in the memory 13 and is circulated in the "twist and invert" loop, the binary word returned to the memory 13 is 01.

The first selector circuit 8 has a left pair of input ports and a right pair of input ports in addition to a pair of output ports and a control port which is connected to the output port 20 of the binary decoder 2. The first selector circuit 8 is arranged with its left pair of input ports connected to the Q1, Q2 output ports of the dual D bistable flip-flop 3 and its right pair of input ports connected to the right pair of output ports of the memory 13.

A second binary decoder 14 has its input ports connected to the output ports of the first selector circuit 8 and has four output ports. The second binary decoder 14 is such that a logic 1 signal appears on only one output port at a time in accordance with a two-bit input code. Each output port of the second binary decoder 14 is arranged to select one of the balance networks 104, 105, 106 and 107 and to connect it to the second transformer 102, of Fig. 1.

Assessment of the transformer loss (THL) is effected by means of an input filter 15 which is arranged to receive the signal passing through the switch 17, the input filter being a narrow-band pass filter having its centre frequency at the oscillator frequency i.e. at around 1500 Hz. The signal passing through the filter 15 is then passed to a precision rectifier 16 which provides the negative rectified value of the signal from the input filter 15. The precision rectifier could be a positive rectifier. The output port of the precision rectifier 16 is connected to one input port of a comparator 18 by way of a long time-constant capacitor-resistor network, and the output of the precision rectifier 16 is connected to the other input port of the comparator 18 by way of a short time-constant capacitor-resistor network. The provision of the long time-constant network at one input port of the comparator 18 permits it to function as a sample-and-hold comparator, since, if the two signals are presented to the comparator 18 in succession with an interval that lies between the long and short time-constants, the comparator 18 output at the arrival of the second signal will be the difference between the signals. The long time-constant network holds the first signal during the presence of the second signal, and the comparator yields the difference in the presence of the second signal. The short time-constant may be zero.

The output port of the comparator 18 is connected to one input port of a two-input port NAND gate 19, the other input port of the NAND gate 19 being connected to the output port of the monostable flip-flop 7. The monostable flip-flop 7 and the NAND gate 19 together act to select the comparator output signal only when it is valid. The output port of the NAND gate 7 is connected to the CLOCK input port of the single D bistable flip-flop 5, which has its Q output port connected to the control port of the second selector circuit 12.

The interaction of the various circuit components just described may be fully understood by considering the operation of the system, which is as follows:—

When the customer's handset is lifted off the hook, the dialling circuits are disconnected, the test oscillator is connected to one input winding of the hybrid transformer, and the control logic system of Fig. 2 is connected to the other input winding of the hybrid transformer. The control circuit then operates to connect the compensating networks in turn to the transformer centre tap and to select the best one before the dialling circuits are reconnected.

When the customer's handset is lifted the first binary decoder provides the output code 1000 because it is always left in this state. The logic 1 on output port 20 from the binary decoder 2 energises the CLOCK input port of the dual D bistable flip-flop 3 to read the contents of the left half of the memory 13 into the flip-flop 3, and the logic 1 is inverted by the first inverter 4 and the resulting logic 0 is applied to the PRESET input port of the single D bistable flip-flop 5 resulting in a logic 0 appearing at the Q output port of the flip-flop 5. The logic 1 at the output port of the flip-flop 5 switches the second selector circuit 12 to enable the Q1 Q2 output signals on the right input ports of the memory 13 which ignores the signals because its $\overline{\text{SAVE}}$ input port is held at logic 1. The logic 0 from output port 21 of the binary decoder 2 goes to the control input port of the first selector circuit 8 which responds by connecting the right output ports of the memory 13 to the second decoder 14 which selects and connects one of the networks to the hybrid transformer. The network connected corresponds to the two-bit code contained in the right-hand side of the memory 13, and the corresponding output signal is fed to the comparator 18 by way of the precision rectifier 16 and the input filter 15. The output port 22 of the decoder 2 provides a logic 0 which is inverted by the second inverter 9 which then applies a logic 1 to the $\overline{\text{SAVE}}$ input port of the memory 13 to lock data out of the memory 13 as mentioned previously.

The decoder 2 is then stepped on by the sequencer 1 to give an output signal 0100. The logic 1 on output port 21 now operates on the first selector circuit 8 to permit the two-bit word held by the dual flip-flop 3 to pass to the second decoder 14 and thereby to connect the network corresponding to this two-bit word to the hybrid transformer. The comparator 18 receives the corresponding signal by way of the precision recifier 16 and the input filter 15. The long time-constant input port of the comparator 18 will have retained the previous input signal and will respond to the new signal very slowly, whereas the previous input signal will have been lost by the

short-time constant input port which will respond rapidly to the new input signal. The comparator therefore provides an output signal corresponding to the difference between the earlier signal and the present signal, and this signal is allowed to pass to the CLOCK input port of the single D flip-flop 5 because the logic 1 on output port 21 of the decoder 2 passes to the monostable flip-flop 7 which then opens the NAND gate 19 providing access to the said CLOCK input port. During this time the memory 13 still locks out data because of the logic 0 on output port 22 of the decoder 2, and the dual flip-flop 3 locks out data because of the logic 0 on the output port 20 of the said decoder.

The Q output port of the single D flip-flop 5 will have a logic level to select the contents of the dual D flip-flop 3 if the later result was better and to select the contents of the right-hand side of the memory 13 if the earlier result was better, for presentation to the output ports of the second selector circuit 12.

The decoder 2 then steps on to provide an output signal 0010, the only effect of which is to open the input ports of the memory 13, since output port 22 of the decoder 2 is now at logic 1. Either the contents of the dual D flip-flop 3 or of the right side of the memory 13 are fed to the right input ports of the memory 13 by way of the second selector circuit 12 and accepted by the memory 13. The right side of the memory 13 is therefore loaded with the better of the two codes originally held in the left and right halves, respectively, of the memory, and as selected by the THL test.

During the period when the output of the decoder 2 is 0010 and its output port 22 is at logic 1, the contents of the left half of the memory 13 become Q2 $\overline{Q1}$ because of the "twist and invert" loop connection between the left half of the memory 13 and the dual D bistable flip-flop 3.

The decoder 2 then steps on to provide an output signal 0001. This is an "idle" output signal which is unused, and the decoder 2 will then step on to 1000. If the decoder 2 is stopped at 1000, the logic 0 on the output port 21 will select the right-hand contents of the memory 13 by way of the first selector circuit 8 for use as the best balance code and the corresponding network will be connected into the system when the test system is disconnected and replaced by the dialling and transmission circuits.

The execution of one cycle results in the selection for the "better" of the two codes held in the memory 13 at the start of the cycle, and the use of the corresponding "better balance" network. However, a "best balance" result can be achieved by executing several cycles in order to test all possibilities in pairs, thereby selecting a "better balance" at each cycle and storing it in the right hand side of the memory 13. The "twist and invert" connection between the left half of the memory 13 and the dual D flip-flop 3 results in the contents of the left half of the memory 13 being changed at each cycle, and the combination acting as a two-bit cyclic counter which calls up each code in turn for comparison with the code held in the right half of the memory 13. The contents of the right half of the memory 13 are then used to select the network to be used.

The system may be used as a single-cycle "better balance" test circuit, in which case it becomes desirable to have a non-volatile memory 13, in order to retain the "better balance" code between calls. A suitable non-volatile memory is the Type MN 9102 4-bit data latch available as an integrated circuit from Plessey Semiconductors. Other non-volatile memory devices using MNOS transistors as memory devices and capable of operating from standard TTL and MOS power supplies would also be suitable.

When the system is used as a multi-cycle test circuit giving "best balance" results, there is no penalty for loss of data from the memory 13 between calls, and a non-volatile memory becomes unnecessary.

The selector circuit of Fig. 3 connects the left pair of input ports to the output port when the control input port is held at logic 1, and connects the right pair of input ports to the output port when the control input port is held at logic 0.

The decoder of Fig. 4 provides a logic 1 output on only one of its output ports at a time in accordance with the two-bit code present at its input ports.

It will be appreciated that the flow-diagram representation of the steps performed by the circuit and shown in Fig. 5, is suitable for implementation by a programmable device, such as a computer, by translation of the flow diagram of Fig. 5 into a language appropriate to the computer. The computer may have a microprocessor as its central processing unit.

CLAIMS

1. Apparatus for compensation of a transmission line, including a plurality of compensating networks having reactive components arranged for connection to the transmission line, and means arranged to measure, periodically, a parameter of the transmission line with one of the networks connected to it and to connect one of the compensating networks to the transmission line according to the value of the parameter.

2. Apparatus for compensation of a transmission line as claimed in claim 1, and including first switch means located between the compensating networks and the transmission line and arranged to connect one of the compensating networks to the transmission line in accordance with the digital code ap-

plied to the first switch.

3. Apparatus for compensation of a transmission line as claimed in claim 2, wherein the means arranged to measure the parameter of the transmission line and to connect one of the compensating networks to the line includes a control circuit which, in operation, provides the digital code for the first switch.

4. Apparatus for compensation of a transmission line as claimed in any one of claims 1 to 3, wherein the means arranged to measure the parameter of the transmission line includes an oscillator, a test circuit, and a second switch.

5. Apparatus for compensation of a transmission line as claimed in claim 4, wherein the test circuit includes a comparator having a long time-constant analogue storage circuit connected to one input port and a short time-constant circuit connected to another input port.

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